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EXAMINER	
SCHNEE, HAL W	

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2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,648	HAMPEL, CRAIG E.	
	Examiner	Art Unit	
	HAL SCHNEE	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :27 May 2004, 6 January 2005, 8 November 2007, 8 August 2008.

DETAILED ACTION

1. Claims 26-49 are pending in this application. Claims 1-25 are cancelled and Claims 26-49 are new by preliminary amendment filed 26 March 2008.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 26-32 and 34-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (U.S. Patent 6,621,496) in view of Kuhne (U.S. Patent 6,188,638).

Regarding Claim 26, Ryan teaches a memory device (figs. 1, 3a, and 3b; col. 3, line 64 – col. 4, line 2) comprising:

a timing signal receive circuit to receive a first timing signal from a memory controller (fig. 3b, drivers connected to pins 304, receiving data strobe DQS {i.e. first timing signal}; col. 5, lines 50-57);

an input buffer to receive write data from the memory controller (fig. 3b, receiver RCVRS, connected to input pins 304; col. 5, lines 50-57);

a data-in register coupled to the first timing signal receive circuit and the input buffer, the data-in register to clock receipt of the write data with the first timing signal (fig. 3b, Input Register; col. 5, lines 58-65);

output circuitry to transmit read data to the memory controller (fig. 3b, Driver connected to pins 304; col. 5, lines 58-65); and

a mode register to store a mode value indicative of memory device operation (fig. 3a, Mode Register 314, shown in more detail in fig. 3c; col. 4, lines 28-31 and col. 6, lines 45-52).

Ryan does not specifically teach wherein when the mode value is set to a first value, the output circuitry to clock the read data with the first timing signal received from the memory controller, and when the mode value is set to a second value, the output circuitry to clock the read data with a second timing signal.

However, Kuhne teaches when the mode value is set to a first value, the output circuitry to clock the read data with the first timing signal received from the memory controller (col. 4, lines 5-11—in the second operating mode {first value of the present claim}, the data strobe signal DQS, received from the memory controller, is used for clocking the read data), and

when the mode value is set to a second value, the output circuitry to clock the read data with a second timing signal (col. 4, lines 5-11—in the first operating mode {second value of the present claim}, the data strobe from the memory controller is not used to clock the read data, indicating that the read data is clocked by a second timing signal, such as system clock CK).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the two operating modes of Kuhne with the memory device and mode register of Ryan to yield the predictable result of when the mode value is set to a first value, the output circuitry to clock the read data with the first timing signal received from the memory controller, and when the mode

value is set to a second value, the output circuitry to clock the read data with a second timing signal. One would be motivated to make this combination for the purpose of providing compatibility with a wider variety of memory systems (as suggested by Ryan, col. 2, lines 51-59).

Regarding Claim 36, Ryan teaches a method of operating a memory device to store data in a memory system (Claim 18), comprising:

receiving a first timing signal from a memory controller (fig. 3b, drivers connected to pins 304, receiving data strobe DQS {i.e. first timing signal}; col. 5, lines 50-57);

receiving write data from the memory controller; transmitting read data to the memory controller (col. 5, lines 50-57); and

clocking the read data corresponding to a stored mode value indicative of memory device operation (col. 4, line 60 – col. 5, line 11).

Ryan does not teach the operation including:

when the mode value is set to a first value, clocking the write data with the first timing signal, and clocking the read data with the first timing signal, and

when the mode value is set to a second value, clocking the write data with the first timing signal, clocking the read data with a second timing signal.

However, Kuhne teaches when the mode value is set to a first value, clocking the write data with the first timing signal, and clocking the read data with the first timing signal, and when the mode value is set to a second value, clocking the write data with the first timing signal, clocking the read data with a second timing signal (col. 4, lines 5-11—in the second operating mode {first value of the present claim}, the data strobe signal DQS, received from the memory

controller, is used for clocking the read data. In the first operating mode {second value of the present claim}, the data strobe from the memory controller is not used to clock the read data, indicating that the read data is clocked by a second timing signal, such as system clock CK. In both modes, write data is clocked by data strobe DQS {the first timing signal}).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the two operating modes of Kuhne with the method of Ryan to yield the predictable result of clocking operation including when the mode value is set to a first value, clocking the write data with the first timing signal, and clocking the read data with the first timing signal, and when the mode value is set to a second value, clocking the write data with the first timing signal, clocking the read data with a second timing signal. One would be motivated to make this combination for the purpose of providing compatibility with a wider variety of memory systems (as suggested by Ryan, col. 2, lines 51-59).

Regarding Claim 43, Ryan teaches a memory device (figs. 1, 3a, and 3b; col. 3, line 64 – col. 4, line 2) comprising:

input circuitry to receive a first timing signal and write data from a memory controller (fig. 3b, drivers and receiver RCVRS connected to pins 304, receiving data strobe DQS {i.e. first timing signal}; col. 5, lines 50-57); and

output circuitry to output read data to the memory controller (fig. 3b, Driver connected to pins 304; col. 5, lines 58-65).

Ryan teaches the memory device having two modes of operation (col. 4, lines 28-31), but does not specifically teach:

wherein in a first mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with the first timing signal, and

in a second mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with a second timing signal.

However, Kuhne teaches wherein in a first mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with the first timing signal, and in a second mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with a second timing signal (col. 4, lines 5-11—in the second operating mode {first value of the present claim}, the data strobe signal DQS, received from the memory controller, is used for clocking the read data. In the first operating mode {second value of the present claim}, the data strobe from the memory controller is not used to clock the read data, indicating that the read data is clocked by a second timing signal, such as system clock CK. In both modes, write data is clocked by data strobe DQS {the first timing signal}).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the two operating modes of Kuhne with the memory device of Ryan to yield the predictable result of

in a first mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with the first timing signal, and in a second mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with a second timing signal. One would be motivated to make this combination for the purpose of providing compatibility with a wider variety of memory systems (as suggested by Ryan, col. 2, lines 51-59).

Regarding Claim 44, Ryan teaches a memory device (figs. 1, 3a, and 3b; col. 3, line 64 – col. 4, line 2) comprising:

input circuitry to receive a first timing signal and write data from a memory controller (fig. 3b, drivers and receiver RCVRS connected to pins 304, receiving data strobe DQS {i.e. first timing signal}; col. 5, lines 50-57); and

output circuitry to output read data to the memory controller (fig. 3b, Driver connected to pins 304; col. 5, lines 58-65).

Ryan teaches the memory device having two modes of operation (col. 4, lines 28-31), but does not specifically teach:

wherein in a first mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses the first timing signal as a phase reference while transmitting the read data, and

in a second mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses a second timing signal as a phase reference while transmitting the read data.

However, Kuhne teaches wherein in a first mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses the first timing signal as a phase reference while transmitting the read data, and in a second mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses a second timing signal as a phase reference while transmitting the read data (col. 4, lines 5-11—in the second operating mode {first value of the present claim}, the data strobe signal DQS, received from the memory controller, is used as a phase reference for clocking the read data. In the first operating mode {second value of the present claim}, the data strobe from the memory controller is not used to clock the read data, indicating that the read data is clocked by a second timing signal, such as system clock CK, used as a phase reference. In both modes, write data is clocked by data strobe DQS {the first timing signal}).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the two operating modes of Kuhne with the memory device of Ryan to yield the predictable result of wherein in a first mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses the first timing signal as a phase reference while transmitting the read data, and in a second mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses a second timing signal as a phase reference while transmitting the read data. One would be motivated to make this combination for

the purpose of providing compatibility with a wider variety of memory systems (as suggested by Ryan, col. 2, lines 51-59).

Regarding Claim 45, Ryan teaches a memory system (col. 6, lines 27-34), comprising a memory controller, the memory controller to generate a first timing signal and to output first data (col. 5, lines 50-57);

a memory module comprising a first memory device having two modes of memory device operation, the first memory device to output second data (figs. 1, 3a, and 3b; col. 3, line 64 – col. 4, line 2);

an interconnect coupling the controller to the memory module, the first memory device to receive the first data over the interconnect and to transmit the second data over the interconnect (fig. 3b, pins 304 of the memory module are connected to an interconnect coupled to the controller); and

a timing signal bus coupling the controller to the memory module, the first memory device to receive the first timing signal over the timing signal bus (fig. 3b; col. 5, lines 50-57—lines connected to data strobe DQS are a timing signal bus for receiving the first timing signal).

Ryan does not specifically teach:

wherein in a first mode of device operation, the first memory device clocks the first data and the second data with the first timing signal, and

in a second mode of device operation, the first memory device clocks the first data with the first timing signal and the second data with a second timing signal.

However, Kuhne teaches wherein in a first mode of device operation, the first memory device clocks the first data and the second data with the first timing signal, and in a second mode

of device operation, the first memory device clocks the first data with the first timing signal and the second data with a second timing signal (col. 4, lines 5-11—in the second operating mode {first mode of device operation of the present claim}, the data strobe signal DQS, received from the memory controller, is used for clocking the read {second} data. In the first operating mode {second mode of device operation of the present claim}, the data strobe from the memory controller is not used to clock the read {second} data, indicating that the second data are clocked by a second timing signal, such as system clock CK. In both modes, write {first} data are clocked by data strobe DQS {the first timing signal}).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the two operating modes of Kuhne with the method of Ryan to yield the predictable result of in a first mode of device operation, the first memory device clocks the first data and the second data with the first timing signal, and in a second mode of device operation, the first memory device clocks the first data with the first timing signal and the second data with a second timing signal. One would be motivated to make this combination for the purpose of providing compatibility with a wider variety of memory systems (as suggested by Ryan, col. 2, lines 51-59).

Regarding Claims 27 and 38, Ryan teaches the mode register is configured to store the mode value responsive to a command from the memory controller (col. 5, lines 22-31).

Regarding Claims 28 and 39, Ryan teaches the memory device coupled to a data bus, wherein the write data is received over the data bus, and the read data is transmitted over the data

bus (fig. 3b, pins 304; col. 5, lines 41-50—the pins are used for both read and write access, indicating that they are connected to a bus).

Regarding Claims 29, 40, and 47, Ryan teaches the memory device coupled to a control and address bus, wherein the memory device is configured to receive over the control and address bus control and address signals from the memory controller (fig. 3a, Control Pins 308; col. 5, lines 58-65).

Regarding Claims 30 and 41, Ryan teaches the control and address signals are received in conjunction with the second timing signal, the second timing signal clocking receipt of the control and address signals (fig. 3a, Control Pins 308; col. 5, lines 58-65—the control and address signals are clocked by system clock CLK, not by the data strobe).

Regarding Claim 31, Ryan does not specifically teach a multiplexer, the multiplexer coupled to the mode register, the multiplexer to provide the first timing signal to the output circuitry when the mode value is set to the first value and to provide the second timing signal to the output circuitry when the mode value is set to the second value.

However, Kuhne teaches a multiplexer, the multiplexer coupled to the mode register, the multiplexer to provide the first timing signal to the output circuitry when the mode value is set to the first value and to provide the second timing signal to the output circuitry when the mode value is set to the second value (fig. 2, Control Device 5; col. 4, lines 15-44—the control device works as a multiplexer, selecting between the two clock signals depending upon the setting of the mode register).

All of the claimed elements were known in Ryan and Kuhne and could have been combined by known methods with no change in their respective functions. It therefore would

have been obvious to a person of ordinary skill in the art at the time of invention to combine the multiplexer of Kuhne with the mode register of Ryan to yield the predictable result of a multiplexer, the multiplexer coupled to the mode register, the multiplexer to provide the first timing signal to the output circuitry when the mode value is set to the first value and to provide the second timing signal to the output circuitry when the mode value is set to the second value. One would be motivated to make this combination for the purpose of implementing the circuitry to select between the clocks as required by the operating modes.

Regarding Claims 32 and 42, Ryan teaches an output buffer, wherein when the mode value is set to the second value, the output buffer to drive the second timing signal as the timing signal for the read data being transmitted from the output circuitry (col. 5, lines 51-56—during a read, the memory device drives the clock signal {second timing signal} as an output strobe).

Regarding Claims 34 and 37, Ryan teaches when the mode value is set to the second value, the memory device transmits the second timing signal to the memory controller (col. 5, lines 51-56—the strobe signal DQS operates bidirectionally, with the memory device transmitting the second timing signal as an output strobe).

Regarding Claim 35, Ryan teaches a data storage array to store the write data, the output circuitry coupled to the data storage array (fig. 3a, memory banks 302; col. 5, lines 32-40).

Regarding Claim 46, Ryan teaches the memory module further comprising: a plurality of dynamic memory random access memory devices (DRAMs), the plurality of DRAMs including the first memory device (fig. 3a, memory banks 302; col. 5, lines 32-40).

4. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (U.S. Patent 6,621,496) in view of Kuhne (U.S. Patent 6,188,638), as applied to Claim 26, above, and further in view of Wu et al. (U.S. 2005/0018494, hereafter "Wu").

Regarding Claim 33, Ryan/Kuhne does not teach when the mode value is set to the first value, the memory device receives the first timing signal continuously from the memory controller. However, Wu teaches a mode in which the memory device receives the a strobe signal (i.e. first timing signal) continuously from a memory controller (fig. 1; ¶ [0025] and Claim 16—when the Continuous_Read signal is high, the data strobe receiver is in a mode in which the first timing signal {i.e. the data strobe} is received continuously).

All of the claimed elements were known in Ryan/Kuhne and Wu and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the continuous receive mode of Wu with the modes of Ryan/Kuhne to yield the predictable result of when the mode value is set to the first value, the memory device receives the first timing signal continuously from the memory controller. One would be motivated to make this combination for the purpose of allowing compatibility with a wider variety of memory controllers.

5. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (U.S. Patent 6,621,496) in view of Kuhne (U.S. Patent 6,188,638), as applied to Claim 45, above, and further in view of Yamaguchi et al. (U.S. 2003/0026161, hereafter "Yamaguchi").

Regarding Claim 48, Ryan/Kuhne does not teach when the first memory device operates in the first mode of device operation, the timing signal bus operates in a unidirectional mode, and

wherein when the first memory device operates in the second mode of device operation, the timing signal bus operates in a bidirectional mode.

However, Yamaguchi teaches a memory device with two modes of operation, wherein in the first mode of device operation, the timing signal bus operates in a unidirectional mode, and wherein when the first memory device operates in the second mode of device operation, the timing signal bus operates in a bidirectional mode (fig. 65; ¶ [0378] - [0379]—in MODE0, the timing signal bus QS operates in a bidirectional mode; in MODE1, but QS operates in a unidirectional mode).

All of the claimed elements were known in Ryan/Kuhne and Yamaguchi and could have been combined by known methods with no change in their respective functions. It therefore would have been obvious to a person of ordinary skill in the art at the time of invention to combine the uni- and bi-directional operation of the timing signal bus of Yamaguchi with the modes of Ryan/Kuhne to yield the predictable result of when the first memory device operates in the first mode of device operation, the timing signal bus operates in a unidirectional mode, and wherein when the first memory device operates in the second mode of device operation, the timing signal bus operates in a bidirectional mode. One would be motivated to make this combination for the purpose of allowing the memory device of Ryan/Kuhne to work with memory controllers that utilize either unidirectional or bidirectional timing signals.

Regarding Claim 49, Ryan/Kuhne teaches when the first memory device operates in the second mode of device operation, the memory device drives the second timing signal onto the timing signal bus (Ryan, col. 5, lines 51-56—the strobe signal DQS operates bidirectionally, with the memory device transmitting the second timing signal as an output strobe).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HAL SCHNEE whose telephone number is (571)270-1918. The examiner can normally be reached on Monday-Friday 8:00 a.m. to 4:30 p.m. E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

HWS 6 October 2008